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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,633	09/30/2003	Muhammed Ayman Shibib	38-7	6066

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Ryan, Mason & Lewis, LLP
90 Forest Avenue
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EXAMINER

TRAN, MINH LOAN

ART UNIT PAPER NUMBER

2826

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/675,633

Applicant(s)

SHIBIB ET AL.

Examiner

Minh-Loan T. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 13-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/30/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-12 in the reply filed on 07/19/2004 is acknowledged. The traversal is on the ground(s) that the apparatus set forth in claims 1 and 10 cannot be made by a process other than and materially different from the process set forth in claim 13, and that the process of claim 13 cannot be used to form a product other than and materially different from the product set forth in claims 1 and 10. Accordingly, the inventions set forth in the subject claims are properly linked to one another and should be considered together." This is not found persuasive because referring to the restriction requirement set forth in the Office Action mailed on 06/15/2004, unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, because the device of Group I invention could be made by a process materially different from that of the Group II invention. For example, the device of claims 1 and 10 require the process steps that form the buried LDD region which is between the gate and the drain region and is spaced laterally from the drain region. Further, the process of forming the device of claims 1 and 10 do not require the steps of removing the shielding structure, removing a portion of an insulating layer under the shielding structure and forming a new shielding structure on a portion of the insulating layer on which the removed shielding structure was formed as recited in the method claims 15-17. Thus, the device set forth in claims 1 and 10 can be made by a process other than and materially different from the process set forth in claim 13, and

that the process of claim 13 can be used to form a product other than and materially different from the product set forth in claims 1 and 10.

The requirement is still deemed proper and is therefore made FINAL.

Information Disclosure Statement

2. The information disclosure statement filed 09/30/2003 has been considered.

Oath/Declaration

3. The oath or declaration filed on 09/30/2003 is acceptable.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the buried LDD region, **of the same conductivity type as that of the source/drain region, being spaced laterally from the drain region** as recited in claims 1 and 10; the shielding structure is electrically connected to the source region as recited in claims 2 and 11; a first insulating layer under the gate and a second insulating layer under the shielding structure are formed of **different thickness in comparison to one another** as recited in claim 4; and the device comprises a **vertical DMOS** as recited in claim 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Note that figures 2, 5, 6 show the buried LDD region 216 (306, 602) isn't spaced laterally from the drain region 208 (314,606); and the insulating layer under the shielding structure 230, (318, 612) and the insulating layer under the gate 210 (316, 610) don't have different thickness in comparison to one another.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in

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the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification and the drawings do not disclose a first insulating layer under the gate and a second insulating layer under the shielding structure are formed of **different thickness in comparison to one another** as recited in claim 4. Note that claim 4 depends on claim 2 which recites the shielding structure is substantially non-overlapping relative to the gate. Figures 2, 5, 6 show the shielding structure is substantially non-overlapping relative to the gate but do not show the thickness difference between the insulating layers under the gate and the shielding structure.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 9-11, "the **buried LDD region being spaced laterally from the drain region**; and a second LDD region of the first conductivity type formed in the buried LDD region" is unclear as to whether it is being referred to a second LDD region of the first conductivity type formed in the buried LDD region and being spaced laterally from the drain region;

Lines 12 and 13, "the second LDD region being self-aligned with the gate and spaced laterally from the gate" is unclear as to how can the second LDD

region be **self-aligned** with the gate and **spaced laterally from the gate**. If the second LDD region is self-aligned with the gate, it can not be spaced laterally from the gate.

In claim 10, lines 10-12, "the **buried LDD region being spaced laterally from the drain region**; and a second LDD region of the first conductivity type formed in the buried LDD region" is unclear as to whether it is being referred to a second LDD region of the first conductivity type formed in the buried LDD region and being spaced laterally from the drain region.

Lines 13 and 14, "the second LDD region being self-aligned with the gate and spaced laterally from the gate" is unclear as to how can the second LDD region be **self-aligned** with the gate and **spaced laterally from the gate**. If the second LDD region is self-aligned with the gate, it can not be spaced laterally from the gate.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 10, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa Akio (JP 2001-15741).

With regard to claims 1, 5, 6, 10, figure 11 of Nakagawa Akio discloses a metal-oxide-semiconductor (MOS) device comprising a p-type semiconductor layer 11; an n-type source region 21 formed in the p-type semiconductor layer 11; an n-type drain region 17 formed in the p-type semiconductor layer 11 and spaced apart from the

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source region 21; a gate 33 formed proximate an upper surface of the p-type semiconductor layer 11 and at least partially between the source and drain regions 21, 17; an n-type buried LDD region 13 formed in the p-type semiconductor layer 11 between the gate 33 and the n-type drain region 17; a p-type second LDD region 19 formed in the n-type buried LDD layer 13 and proximate the upper surface of the semiconductor layer 11, the p-type second LDD region 19 being spaced laterally from the gate 33 such that the gate 33 is non-overlapping relative to the p-type second LDD region 19, and the p-type second LDD region 19 being spaced laterally from the n-type drain region 17.

With regard to claims 2 and 11, figure 11 of Nakagawa Akio discloses a shielding structure 45 formed proximate the upper surface of the p-type semiconductor layer 11 and at least partially between the gate 33 and the drain region 17; the shielding structure 45 being electrically connected to the source region 21 through the source electrode 27; the shielding structure 45 being spaced laterally from the gate 33 and being substantially non-overlapping relative to the gate 33.

With regard to claim 3, Applicant's claim 3 does not distinguish over the Nakagawa Akio's reference regardless of the process used to form the shielding structure because only the final product is relevant, not the process of making such as "formed substantially concurrently with the gate".

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In*

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re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa Akio (JP 2001-15741).

Figure 11 of Nakagawa Akio does not disclose the device is a vertical DMOS and the buried LDD is formed in the semiconductor layer at a depth in a range from about 0.5 micron to about 2 micron and the second LDD region is formed in the semiconductor layer at a depth in a range from about 0.05 micron to about 0.5 micron. Although Nakagawa Akio does not teach exact the type of the device and the depths of the buried LDD region and the second LDD region as that claimed by Applicant, the type and the depth differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It

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appears that these changes produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416, *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Circ. 1990).

Allowable Subject Matter

9. Claims 9 and 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh-Loan T. Tran whose telephone number is (571) 272-1922. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mlt



Minh-Loan T. Tran
Primary Examiner
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